DAC

Docket No. A-67736-1/MSS/TJH
Dorsey Matter No.: 463035-19

CERTIFICATE OF MAIL UNDER 37 C.F.R. 1.08

I hereby certify that this paper (along with any referred to as being attached or enclosed) is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Mail Stop Petition, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on October 3, 2003.

Signed: _____
Laura Lee Mosier

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: SAVAGE *et al.*		Examiner:	FOX, Charles A.
Application No.	09/767,659	Art Unit:	3652
Filed:	January 22, 2001		
For:	Semiconductor Wafer Processing System with Vertically-Stacked Process Chambers and Single-Axis Dual Wafer Transfer System	Date:	October 3, 2003

PETITION TO WITHDRAW HOLDING OF ABANDONMENT UNDER 37 CFR 1.181(a) TRANSMITTAL

Mail Stop Petition
P.O. Box 1450
Commissioner for Patents
Alexandria, VA 22313-1450

Sir:

Please find enclosed the following documents relating to the above-identified patent application:

- X Petition to Withdraw Holding of Abandonment under 37 CFR 1.181 (a), 2 pages;
- X Copy of Notice of Abandonment dated September 4, 2003, 2 pages;
- X Copy of previously filed Request for Continued Examination Transmittal, 1 page;
- X Copy of previously filed Amendment after Final in response to Examiner's Official Action of December 31, 2002, 9 pages;
- X Copy of previously submitted Check No. 5569 for RCE filing fee of $860 and our return Post Card; and
- X Copy of our returned post card with receipt stamp dated May 6, 2003 by the U.S. Patent and Trademark for the above listed items.

Applicant submits that a petition under 37 CFR 1.181(a) does not require a fee. However, the Commissioner is authorized to charge any additional fees to Deposit Account No. 50,2319 (Order No. A-67736-1/MSS/TJH).

Respectfully submitted,

By _____
Tianjun Hou
Reg. No. 51,821

Dorsey & Whitney LLP
4 Embarcadero Center, Suite 3400
San Francisco, CA 94111-4187
Telephone: (650) 494-8700
Facsimile: (650) 494-8771

CERTIFICATE OF MAIL UNDER 37 C.F.R. 1.08

I hereby certify that this paper (along with any referred to as being attached or enclosed) is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Mail Stop Petition, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on October 3, 2003.

Signed: *Laura Lee Mosier*

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: SAVAGE *et al.*		Examiner:	FOX, Charles A.
Application No.	09/767,659	Art Unit:	3652
Filed:	January 22, 2001		
For:	Semiconductor Wafer Processing System with Vertically-Stacked Process Chambers and Single-Axis Dual Wafer Transfer System	Date:	October 3, 2003

PETITION TO WITHDRAW HOLDING OF ABANDONMENT UNDER 37 CFR 1.181(a)

Mail Stop Petition
P.O. Box 1450
Commissioner for Patents
Alexandria, VA 22313-1450

Sir:

Applicant received a Notice of Abandonment mailed September 4, 2003, a copy of which is attached. In the Notice, the Examiner stated that a proposed reply was received on April 7, 2003 but it did not constitute a proper reply under 37 CFR 1.113(a) to the final rejection. Applicant respectfully submits that the holding of abandonment is improper and hereby petitions to withdraw.

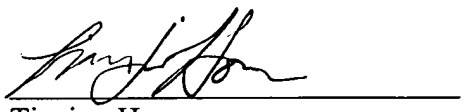
In a final Office Action in the above application mailed on December 31, 2002, the Examiner rejected pending Claims 19-24 over the prior art. Applicant filed an Amendment After Final on March 31, 2003, in which Claims 19 and 24 were amended and new Claims 25-26 were added. In an Advisory Action mailed April 22, 2003, the Examiner did not enter the Amendment and stated that the amendment to Claims 19 and 24 introduced new issues, which is not proper after a final rejection has been issued.

On April 29, 2003, Applicant filed a Request for Continued Examination ("RCE") for this application with RCE filing fee $860 and one month extension fee. Together with the RCE, Applicant submitted a copy of the Amendment After Final filed on March 31, 2003 as submission required under 37 CFR 1.114. A copy of the RCE, the Amendment After Final, the check in amount $860, and the returned post card with the USPTO stamp on it is attached with this petition as evidence showing that Applicant deposited the necessary documents with the U.S. Postal Service on April 29, 2003 and the PTO received the documents on May 6, 2003.

Under 37 CFR 1.114, an applicant may file a RCE after prosecution in the application is closed. Applicant properly filed a RCE under 37 CFR 1.114 with a submission and sufficient fee on April 29, 2003. Under MPEP 706.07(h), the Patent Office should enter any previously filed unentered amendments and amendments filed with the RCE, and continues prosecution of the application. Therefore, Applicant respectfully submits that the holding of abandonment of the present application is improper and hereby petitions to withdraw.

Applicant submits that a petition under 37 CFR 1.181(a) does not require a fee. However, the Commissioner is authorized to charge any additional fees to Deposit Account No. 50,2319 (Order No. A-67736-1/MSS/TJH).

Respectfully submitted,



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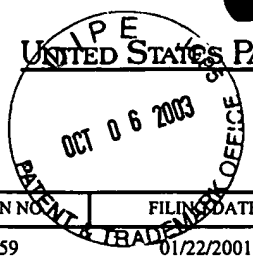
UNITED STATES PATENT AND TRADEMARK OFFICE



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/767,659	01/22/2001	Richard N. Savage	A-67736-1/AJT/MSS	2896

7590 09/04/2003

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EXAMINER
FOX, CHARLES A

ART UNIT	PAPER NUMBER
3652	

DATE MAILED: 09/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

File A-67736-1 Atty AJT/MSS/TJH

Due Date _____

Type _____ Refs _____

Notice of Abandonment

Application No.	Applicant(s)	
09/767,659	SAVAGE ET AL.	
Examiner	**Art Unit**	
Charles A. Fox	3652	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

This application is abandoned in view of:

1. ☒ Applicant's failure to timely file a proper reply to the Office letter mailed on *31 December 2002*.
   (a) ☐ A reply was received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the period for reply (including a total extension of time of _____ month(s)) which expired on _____.
   (b) ☒ A proposed reply was received on *April 7, 2003*, but it does not constitute a proper reply under 37 CFR 1.113 (a) to the final rejection.

   (A proper reply under 37 CFR 1.113 to a final rejection consists only of: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114).
   (c) ☐ A reply was received on _____ but it does not constitute a proper reply, or a bona fide attempt at a proper reply, to the non-final rejection. See 37 CFR 1.85(a) and 1.111. (See explanation in box 7 below).
   (d) ☐ No reply has been received.

2. ☐ Applicant's failure to timely pay the required issue fee and publication fee, if applicable, within the statutory period of three months from the mailing date of the Notice of Allowance (PTOL-85).
   (a) ☐ The issue fee and publication fee, if applicable, was received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the statutory period for payment of the issue fee (and publication fee) set in the Notice of Allowance (PTOL-85).
   (b) ☐ The submitted fee of $_____ is insufficient. A balance of $_____ is due.

   The issue fee required by 37 CFR 1.18 is $_____. The publication fee, if required by 37 CFR 1.18(d), is $_____.
   (c) ☐ The issue fee and publication fee, if applicable, has not been received.

3. ☐ Applicant's failure to timely file corrected drawings as required by, and within the three-month period set in, the Notice of Allowability (PTO-37).
   (a) ☐ Proposed corrected drawings were received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the period for reply.
   (b) ☐ No corrected drawings have been received.

4. ☐ The letter of express abandonment which is signed by the attorney or agent of record, the assignee of the entire interest, or all of the applicants.

5. ☐ The letter of express abandonment which is signed by an attorney or agent (acting in a representative capacity under 37 CFR 1.34(a)) upon the filing of a continuing application.

6. ☐ The decision by the Board of Patent Appeals and Interference rendered on _____ and because the period for seeking court review of the decision has expired and there are no allowed claims.

7. ☐ The reason(s) below:

EILEEN D. LILLIS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 3600

Petitions to revive under 37 CFR 1.137(a) or (b), or requests to withdraw the holding of abandonment under 37 CFR 1.181, should be promptly filed to minimize any negative effects on patent term.

REQUEST FOR CONTINUED EXAMINATION (RCE) TRANSMITTAL

This is a Request for Continued Examination (RCE) under 37 C.F.R. § 1.114 of the above-captioned application.

Application Number	09/767,659
Filing Date	January 22, 2001
First Named Inventor	Richard N. SAVAGE
Group Art Unit	3652
Examiner Name	FOX, Charles A.
Attorney Docket No.	A-67736-1/MSS/TJH

COPY

OIPE OCT 06 2003 PATENT & TRADEMARK OFFICE JC968

MAIL STOP RCE
Commissioner for Patent
P.O. Box 1450
Alexandria, VA 22313-1450

CERTIFICATE OF MAIL (37 CFR 1.8(a))

I hereby certify that this paper (along with any referred to as being attached or enclosed) is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: MAIL STOP RCE, Commissioner for Patent, P.O. Box 1450, Alexandria, VA 22313-1450 on April 29, 2003

Signed: *Laura Lee Mosier*

1. Submission required under 37 C.F.R. § 1.114

a. ☒ Previously submitted

i. ☒ Consider the amendment(s)/reply under 37 C.F.R. § 1.116 previously filed on March 31, 2003 (Any unentered amendment(s) referred to above will be entered.)

ii. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

iii. ☐ Other:

b. ☒ Enclosed

i. ☐ Amendment/Reply

ii. ☐ Affidavit(s)/Declaration(s)

iii. ☐ Information Disclosure Statement (including Form PTO-1449 and References)

iv. ☒ Other: **Copy of the unentered amendment filed on March 31, 2003.**

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2. Miscellaneous

a. ☐ Suspension of action on the above-captioned application is requested under 37 C.F.R. § 1.103(c) for a period of _____ months. (Period of suspension shall not exceed three months; Fee under 37 C.F.R. § 1..17(i) required.)

b. ☐ Other:

3. Fees

The RCE fee under 37 C.F.R. § 1.17(e) is required by 37 C.F.R. § 1.114 when the RCE is filed.

a. ☒ The Fees are calculated as follows:

			AMOUNT	☒ Large Entity	☐ Small Entity
i.	☒	RCE BASIC FEE	$ 750.00	$ 750.00	$ 375.00
ii.	☒	EXTENSION FEES	$ 110.00	One-Month $ 110.00 Two-Month 410.00 Three-Month 930.00 Four-Month 1450.00 Five-Month 1970.00	$ 55.00 205.00 465.00 725.00 985.00
iii.	☐	OTHER	$	$ 18.00	$ 9.00

b. ☒ Check in the amount of $ 860.00 is enclosed. The Commissioner is hereby authorized to charge any variance between the amount enclosed and the Patent Office charges to **Deposit Account No. 50-2319 (A-67736-1/MSS/TJH(463035-19))**.

c. ☐ The Commissioner is hereby authorized to charge the fees as indicated above, charge any variance or credit any overpayments, to **Deposit Account No. 50-2319.**

SUBMITTED BY			Complete (if applicable)	
Typed or Printed Name	Tianjun Hou		Registration No.	51,821
Signature		Date	April 29, 2003	

1056627

CERTIFICATE OF MAIL UNDER 37 C.F.R. 1.10

I hereby certify that this paper (along with any referred to as being attached or enclosed) is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Box AF, Assistant Commissioner for Patents, Washington, D.C. 20231 on March 31, 2003.

Signed: /Laura Lee Mosier/

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: SAVAGE *et al.*	Examiner: FOX, Charles A.
Application No. 09/767,659	Art Unit: 3652
Filed: January 22, 2001	Date: March 31, 2003
For: Semiconductor Wafer Processing System with Vertically-Stacked Process Chambers and Single-Axis Dual Wafer Transfer System	

AMENDMENT AFTER FINAL

Box AF
Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

This Amendment is responsive to the final Office Action mailed December 31, 2002. Please amend the application as follows:

In the Claims:

Please amend claims 19 and 24 to read as shown:

19. (Amended) A method of semiconductor wafer processing comprising the steps of:

providing a multi-chamber module including a plurality of vertically-stacked semiconductor wafer process chambers;

providing a loadlock chamber for each of the vertically-stacked semiconductor wafer process chambers, wherein each loadlock chamber having a transfer arm including an upper wafer shelf for carrying unprocessed wafers and a lower wafer shelf for carrying processed wafers, and a semiconductor wafer process chamber;

simultaneously transferring a processed wafer and an unprocessed wafer between said loadlock chamber and said respective process chamber.

24. (Amended) A method of semiconductor wafer processing comprising the steps of:

providing an atmospheric front end unit including a front end robot for transporting a semiconductor wafer, a multi-chamber module including a plurality of vertically-stacked semiconductor wafer process chambers, a loadlock chamber for each semiconductor wafer process chamber, and a wafer transfer apparatus for each loadlock chamber, each said loadlock chamber and each said wafer transfer apparatus dedicated to a respective wafer process chamber;

transporting a wafer between said atmospheric front end unit and one of said loadlock chambers via said robot; and

simultaneously transferring a processed and an unprocessed wafer between said one loadlock chamber and a respective wafer process chamber via said wafer transfer apparatus.

Please add claims 25 and 26 to read as shown:

25. (New) The method according to claim 19 wherein the simultaneous transferring is performed by a single-axis wafer transfer arm capable of providing an extended position and a home position.

26. (New) The method according to claim 24 wherein the simultaneous transferring is performed by a single-axis wafer transfer arm capable of providing an extended position and a home position.

REMARKS

This amendment is submitted in response to the Office Action dated December 31, 2002. Claims 19 and 24 are amended. New claims 25 and 25 are added. Support for this amendment and addition are found in the specification and drawings. Claims 19-26 are pending in this application.

Claim Rejections under 35 U.S.C. 102:

Claim 24 is rejected under 35 U.S.C. 102 as being anticipated by U.S. Patent No. 6,053,980 to Suda et al (hereafter "Suda"). Applicant respectfully traverses the rejection.

A claim is anticipated under 35 U.S.C. 102 only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference. Applicant respectfully submits that Suda does not teach each and every element of claim 24.

Applicant amends claim 24 of the invention by adding *simultaneously transferring a processed and an unprocessed* wafer between one loadlock chamber and a respective wafer process chamber via a wafer transfer apparatus.

As amended, claim 24 of the invention now comprises the following steps:

providing an atmospheric front end unit including a front end robot for transporting a semiconductor wafer, a multi-chamber module including a plurality of vertically-stacked semiconductor wafer process chambers, a loadlock chamber for each semiconductor wafer process chamber, and a wafer transfer apparatus for each loadlock chamber, each said loadlock chamber and each said wafer transfer apparatus dedicated to a respective wafer process chamber;

transporting a wafer between said atmospheric front end unit and one of said loadlock chambers via said robot; and

simultaneously transferring a processed and an unprocessed wafer between said one loadlock chamber and a respective wafer process chamber via said wafer transfer apparatus.

Suda teaches a substrate processing apparatus comprising a substrate transfer section, a plurality of modules, and a substrate transfer robot for transferring substrates to the plurality of modules. See Suda Abstract and Fig. 1. Suda does not teach *simultaneously transferring a processed and an unprocessed* wafer between one loadlock chamber and a respective wafer process chamber via a wafer transfer apparatus.

Further, Suda does not teach transporting a wafer between the atmospheric front end unit and one of the loadlock chambers via a robot, and transferring the wafer between the loadlock chamber and a respective wafer process chamber via the wafer transfer apparatus including a transfer arm. In Suda, the wafer is transferred first from a cassette loader chamber 10 to a load lock chamber 52, then from the load lock chamber to a transfer chamber 54, and finally from the transfer chamber 54 to a process chamber 56. Suda does not teach transferring a wafer between *an atmospheric front end unit* and *a load lock chamber, and then between the load lock chamber and a process chamber* as recited in claim 24 of the present invention.

Reconsideration of the rejections of claim 24 under 35 U.S.C. 102 is therefore respectfully requested.

Claim Rejections under 35 U.S.C. 103:

Claims 19-21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,073,366 to Aswad (hereafter "Aswad") in view of U.S. Patent No. 5,989,346 to Hiroki (hereafter "Hiroki").

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Aswad in view of U.S. Patent No. 5,695,568 to Sinha et al (hereafter "Sinha").

Applicant respectfully traverses these rejections.

To establish a prima facie case of obviousness under 35 U.S.C. 103(a), first, there must be some suggestion or motivation, whether in the references themselves, or in the knowledge generally available to one of ordinary skill in the art to modify the reference teaching. Second, there must be a reasonable expectation of success. Third, the prior art references must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. Applicant respectfully submits that a prima facie case of obviousness is not established.

Applicant amends claim 19 by adding providing *a multi-chamber module including a plurality of vertically-stacked semiconductor wafer process chambers*, and providing *a loadlock chamber for each of the vertically-stacked semiconductor wafer process chambers*, wherein each loadlock chamber having a transfer arm including an upper wafer shelf for carrying unprocessed wafers and a lower wafer shelf for carrying processed wafers, and a semiconductor wafer process chamber. As amended, claim 19 recites *simultaneously* transferring a processed wafer and an unprocessed wafer between one loadlock chamber and a *respective* process chamber.

Aswad teaches a wafer handler 20 or Bernoulli wand for picking up wafers as shown in Figures 6a-c. In particular, Aswad teaches a wafer handler 20 including pick up arms 24 and 26. In operation, pick up arm 26 translate toward load lock chamber 120 in one direction to pick up a wafer, *then* pick up arm 24 translate toward a processing chamber in an opposite direction to place the wafer on a susceptor 168. Aswad does not teach *transferring processed and unprocessed wafers simultaneously* between the loadlock chamber and process chamber by a

transferring arm that has an upper wafer shelf for carrying unprocessed wafers and a lower wafer shelf for carrying processed wafers.

Hiroki teaches a semiconductor processing apparatus comprising an external transfer mechanism 20 for transferring substrates between a cassette and a loadlock chamber. In particular, the external transfer mechanism has first and second arms defining first and second support surfaces each of which can support one substrate and capable of vertically moving relative to each other. See Hiroki Abstract and Figure 3. However, Hiroki does not teach providing *a multi-chamber module including a plurality of vertically-stacked semiconductor wafer process chambers.* Nor does Hiroki teach providing *one loadlock chamber for each of the vertically-stacked semiconductor wafer process chambers.* In contrast, Hiroki teaches away from the present invention by using one transferring mechanism for at least three process chambers. See FIG. 2 of Hiroki. One advantage of providing one loadlock chamber for each of the process chambers according to the present invention is that it greatly simplifies the path of each wafer into the process chambers and reduces wafer loading/unloading time for each process chamber. One advantage of providing a multi-chamber module including a plurality of vertical-stacked process chambers is to minimize the system's footprint.

Moreover, neither Hiroki nor Aswad teach transferring two wafers, unprocessed and processed, by a simple single-axis transfer arm, as recited in newly added claims 25 and 26 of the present invention. To the contrary, Hiroki teaches a complicated multi-axis transfer mechanism (see Col. 7, lines 30-40 of Hiroki) which the present invention is designed to eliminate. The fact that each process chamber is provided with one loadlock chamber according to the present invention makes possible to use a single-axis transfer arm to simultaneously transfer processed and unprocessed wafers between the loadlock and process chambers, which greatly reduces the manufacturing cost for the system.

There is no motivation for one of ordinary skill in the art to combine Aswad and Hiroki, either from the explicit or implicit teaching or suggestion of these references themselves, or from the knowledge of those of skill in the art, or from the nature of the problem to be solved. Even assuming one of ordinary skills combines Aswad and Hiroki, the combination cannot arrive at the semiconductor processing method as recited in claim 19 of the present invention because neither of the cited references teach or suggest providing a multi-chamber module including a

plurality of vertically-stacked process chambers, and providing one loadlock chamber for each of the vertically-stacked process chambers.

Reconsideration of the rejections of claims 19 under 35 U.S.C 103(a) is therefore respectfully requested.

Claim 20-23 recite further limitations to claim 19, these dependent claims are therefore allowable for at least the same reasons as for claim 19.

In addition, claim 21 of the present invention recites a further step of transferring the processed wafer from the lower wafer shelf to *a cooling plate below the transfer arm within the loadlock chamber*. Aswad does not teach providing a cooling plate under the transfer arm and transferring the processed wafer to the cooling plate. Rather, Aswad teaches cooling stations 46 and 48 disposed *adjacent to* the wafer handler 20, not under the transfer arm within the loadlock chamber as recited in claim 21 of the present invention.

Furthermore, claim 22 of the present invention recites further steps of:

transporting said unprocessed wafer on said upper wafer shelf from said loadlock chamber to said process chamber;

transferring said unprocessed wafer from said upper wafer shelf to a wafer chuck mounted in said semiconductor wafer chamber; and

translating said wafer chuck from a retracted position, past a chemical vapor deposition injector mounted in said semiconductor wafer process chamber, to an extended position, whereby an unprocessed wafer is processed into a processed wafer.

Sinha teaches a chemical vapor deposition chamber including a substrate edge protection system. In particular, Sinha teaches *upwardly raising the wafer for processing, and downwardly lowing the wafer for loading unprocessed wafer and unloading processed wafer, through a heater plate.* See Sinha Col. 4, lines 32-50. However, Sinha does not teach or suggest *translating the wafer chuck from a retracted position, past a chemical vapor deposition injector* mounted in the semiconductor wafer process chamber, to an extended position, whereby an unprocessed wafer is processed into a processed wafer, as recited in claim 22 of the present invention.

Moreover, claim 23 of the invention recites further steps prior to the simultaneously transferring step:

receiving a first unprocessed wafer on the transfer arm;

transferring the first unprocessed wafer to the process chamber;

concurrently processing the first unprocessed wafer into a first processed wafer and receiving a second unprocessed wafer on the transfer arm; and

retrieving the first processed wafer by the transfer arm while holding the second unprocessed wafer on the transfer arm.

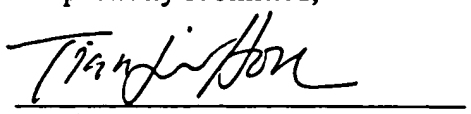
Neither Aswad nor Hiroki teach or suggest these additional steps. Aswad does not teach or suggest retrieving the first processed wafer by the transfer arm while holding the second unprocessed wafer on the transfer arm. Hiroki teaches that a processed substrate is loaded and an unprocessed substrate unloaded at a same time in the loadlock chamber, or a processed substrate is unloaded and an unprocessed substrate loaded in the cassette at a same time. However, Hiroki does not teach or suggest retrieving the first processed wafer by the transferred arm while holding the second unprocessed wafer on the transfer arm.

The newly added claims 25 and 26 recite that the simultaneous transferring step is performed by a single-axis wafer transfer arm capable of providing an extended position and a home position. As stated above, this is advantageous because it greatly reduces the manufacturing costs for a complicated multi-axis transfer arm.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "Version with markings to show changes made".

Based on the foregoing, Applicant respectfully submits that the application is now in condition for allowance. If any matters can be resolved by telephone, the Examiner is invited to call the undersigned attorney at the telephone number listed below. The Commissioner is authorized to charge any additional fees to Deposit Account No. 50,2319 (Order No. A-67736-1/MSS/TJH).

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Please amend the claims as follows. All pending claims are listed below, whether amended or not, for the Examiner's convenience.

19. (Amended) A method of semiconductor wafer processing comprising the steps of:

providing a multi-chamber module including a plurality of vertically-stacked semiconductor wafer process chambers;

providing a loadlock chamber for each of the vertically-stacked semiconductor wafer process chambers, wherein each loadlock chamber having a transfer arm including an upper wafer shelf for carrying unprocessed wafers and a lower wafer shelf for carrying processed wafers, and a semiconductor wafer process chamber;

simultaneously transferring a processed wafer and an unprocessed wafer between said loadlock chamber and said respective process chamber.

20. (Unchanged) A method of semiconductor wafer processing according to claim 19 further comprising the step:

evacuating said loadlock chamber prior to simultaneously transferring a processed wafer and an unprocessed wafer between said loadlock chamber and said process chamber.

21. (Unchanged) A method of semiconductor wafer processing according to claim 19, further includes providing a cooling plate below the transfer arm within said loadlock chamber, said method further comprising:

transferring said processed wafer from said lower wafer shelf to said cooling plate.

22. (Unchanged) A method of semiconductor wafer processing according to claim 21 further comprising;

transporting said unprocessed wafer on said upper wafer shelf from said loadlock chamber to said process chamber;

transferring said unprocessed wafer from said upper wafer shelf to a wafer chuck mounted in said semiconductor wafer chamber,

translating said wafer chuck from a retracted position, past a chemical vapor deposition injector mounted in said semiconductor wafer process chamber, to an extended position, whereby an unprocessed wafer is processed into a processed wafer.

23. (Unchanged) A method of semiconductor wafer processing according to claim 19 further comprising the steps prior to the simultaneously transferring step:

receiving a first unprocessed wafer on the transfer arm;

transferring said first unprocessed wafer to said process chamber;

concurrently processing said first unprocessed wafer into a first processed wafer and receiving a second unprocessed wafer on the transfer arm; and

retrieving said first processed wafer by said transfer arm while holding said second unprocessed wafer on said transfer arm.

24. (Amended) A method of semiconductor wafer processing comprising the steps of:

providing an atmospheric front end unit including a front end robot for transporting a semiconductor wafer, a multi-chamber module including a plurality of vertically-stacked semiconductor wafer process chambers, a loadlock chamber for each semiconductor wafer process chamber, and a wafer transfer apparatus for each loadlock chamber, each said loadlock chamber and each said wafer transfer apparatus dedicated to a respective wafer process chamber;

transporting a wafer between said atmospheric front end unit and one of said loadlock chambers via said robot; and

<u>simultaneously</u> transferring [the] <u>a processed and an unprocessed</u> wafer between said one loadlock chamber and a respective wafer process chamber via said wafer transfer apparatus.

25. (New) The method according to claim 19 wherein the simultaneous transferring is performed by a single-axis wafer transfer arm capable of providing an extended position and a home position.

26. (New) The method according to claim 24 wherein the simultaneous transferring is performed by a single-axis wafer transfer arm capable of providing an extended position and a home position.

(1052068)

COPY

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Palo Alto, CA 94304-1017

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4/29/2003

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File No.: A-67736-1/5702/TJH	U.S. Application No. 09/767,659	Filing Date: January 22, 2001
Date Due: April 30, 2003	Date Mailed: April 29, 2003	Express Mail No.: n/a
Applicant: Richard N. SAVAGE et al.		ASML
Entitled: Semiconductor Wafer Processing system with Vertically-Stacked Process Chambers and Single-Axis Dual-Wafer Transfer System		

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[X] RCE Transmittal, 1 page; [X] Copy of previously filed Response to pending OA, dated March 31, 2003; 9 pages; [X] Check No. 5569 for $860 RCE filing fees & one month extension fee (LARGE ENTITY) [X] and this postcard.	

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